SP5055

2.6GHz Bidirectional I²C BUS Controlled Synthesiser

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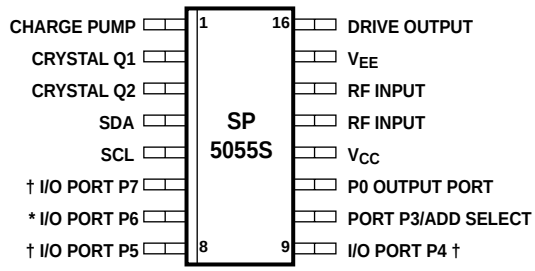
The SP5055 is a single chip frequency synthesiser designed for TV tuning systems. Control data is entered in the standard I²C BUS format. The device contains 4 addressable current limited outputs and 4 addressable Bi-Directional open collector ports one of which is a 3 bit ADC. The information on these ports can be read via the I²C BUS. The device has one fixed I²C BUS address and 3 programmable addresses, programmed by applying a specific input voltage to one of the current limited outputs. This enables 2 or more synthesisers to be used in a system.

FEATURES

- Complete 2.6GHz Single Chip System
- Programmable via I²C BUS
- Low power consumption (5V 65mA)
- Low Radiation
- Phase Lock Detector
- Varactor Drive Amp Disable
- 6 Controllable Outputs, 4 Bi-Directional
- 5 Level ADC
- Variable I²C BUS Address For Multi Tuner Applications
- Full ESD Protection*

* Normal ESD handling procedures should be observed.

Ordering Information
SP5055GS/KG/MPAS (Tubes)
SP5055GS/KG/MPAD (Tape & Reel)
16lead minature plastic package



† = Logic level I/O
* = 3-bit ADC input

MP16

Fig. 1 Pin connections – top view

APPLICATIONS

- Satellite TV
- High IF Cable Tuning Systems

ELECTRICAL CHARACTERISTICS

T_{amb} = -20°C to +80°C, V_{CC} = +4.7V to 5.3V.
These Characteristics are guaranteed by either production test or design. They apply within the specified ambient temperature and supply voltage unless otherwise stated. Reference frequency = 4MHz unless otherwise stated.

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply current	12		65	80	mA	V_{CC} = 5V
Prescaler input voltage	13, 14	50		300	mV_{RMS}	500MHz to 2.6GHz Sinewave
Prescaler input voltage	13, 14	100		300	mV_{RMS}	120MHz, see Fig. 5
Prescaler input impedance	13, 14		50		Ω	
Prescaler input capacitance			2		pF	
SDA, SCL						
Input high voltage	4, 5	3		5.5	V	
Input low voltage	4, 5	0		1.5	V	
Input high current	4, 5			10	µA	Input voltage = V_{CC}
Input low current	4, 5			-10	µA	Input voltage = 0V
Leakage current	4, 5			10	µA	When V_{CC} = 0V
SDA						
Output voltage	4			0.4	V	I_{sink} = 3mA
Charge pump current low	1		±50		µA	Byte 4, bit 2 = 0, pin 1 = 2V
Charge pump current high	1		±170		µA	Byte 4, bit 2 = 1, pin 1 = 2V
Charge pump output leakage current	1			±5	nA	Byte 4, bit 4 = 1, pin 1 = 2V
Charge pump drive output current	16	500			µA	$V_{pin\ 16}$ = 0·7V
Charge pump amplifier gain			6400			
Recommended crystal series resistance		10		200	Ω	
Crystal oscillator drive level	2		80		mVp-p	
Crystal oscillator negative resistance	2	750			Ω	
Output Ports						
P0, P3 sink current	10, 11	0.7	1	1.5	mA	V_{OUT} = 12V
P0, P3 leakage current	10, 11			10	µA	V_{OUT} = 13·2V
P4-P7 sink current	9-6	10			mA	V_{OUT} = 0.7V
P4-P7 leakage current	9-6			10	µA	V_{OUT} = 13·2V
Input Ports						
P3 input current high	10			+10	µA	$V_{pin\ 10}$ = 13.2V
P3 input current low	10			-10	µA	$V_{pin\ 10}$ = 0V
P4,P5,P7 input voltage low	9,8,6			0.8	V	
P4,P5,P7 input voltage high	9,8,6	2.7			V	
P6 input current high	7			+10	µA	See Table 3 for ADC Levels
P6 input current low	7			-10	µA	

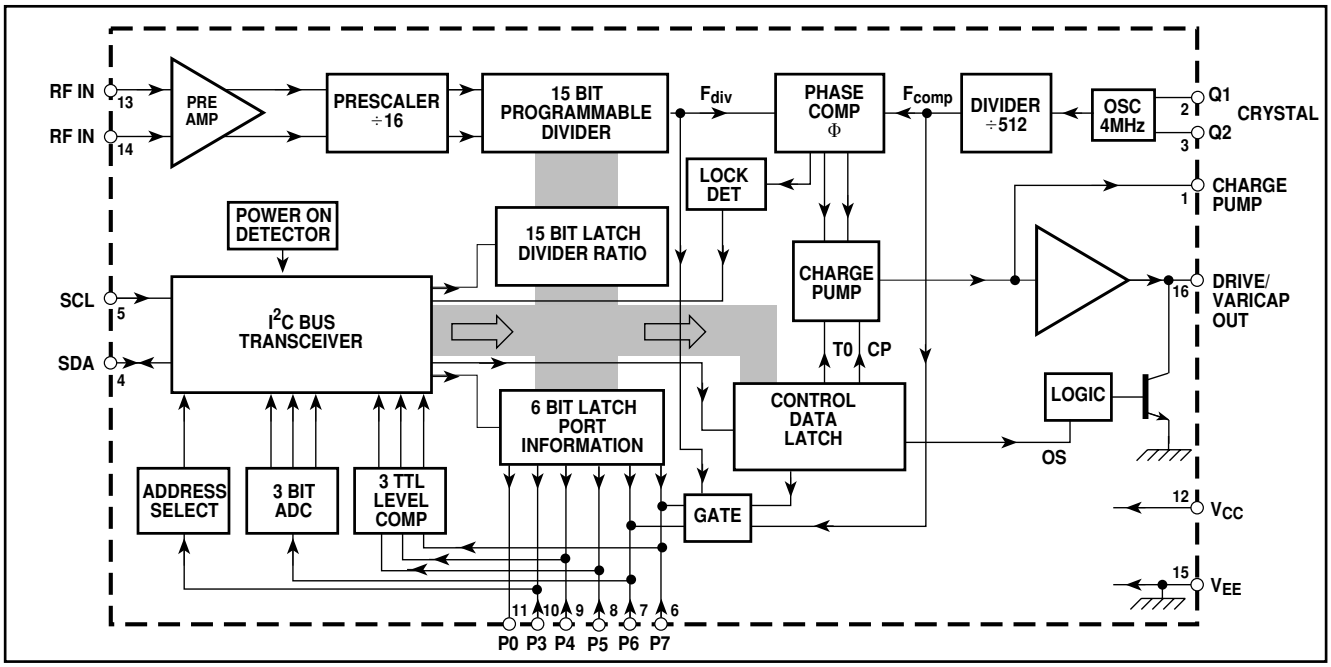


Fig. 2 Block diagram

FUNCTIONAL DESCRIPTION

The SP5055 is programmed from an I²C BUS. Data and Clock are fed in on the SDA and SCL lines respectively as defined by the I²C BUS format. The synthesiser can either accept new data (write mode) or send data (read mode). The Tables in Fig. 3 illustrate the format of the data. The device can be programmed to respond to several addresses, which enables the use of more than one synthesiser in an I²C Bus system. Table 4 shows how the address is selected by applying a voltage to P3. The last bit of the address byte (R/W) sets the device into read mode if it is high and write mode if it is low. When the SP5055 receives a correct address byte it pulls the SDA line low during the acknowledge period and during following acknowledge periods after further data bytes are programmed. When the SP5055 is programmed into the read mode the controlling device accepting the data must pull down the SDA line during the following acknowledge period to read another status byte.

WRITE MODE (FREQUENCY SYNTHESIS)

When the device is in the write mode Bytes 2 + 3 select the synthesised frequency while bytes 4 + 5 select the output port states and charge pump information.

Once the correct address is received and acknowledged, the first Bit of the next Byte determines whether that byte is interpreted as byte 2 or 4, a logic 0 for frequency information and a logic 1 for charge pump and output port information. Additional data bytes can be entered without the need to re-address the device until an I²C stop condition is recognised. This allows a smooth frequency sweep for fine tuning or AFC purposes.

If the transmission of data is stopped mid-byte (i.e., by another device on the bus) then the previously programmed byte is maintained.

Frequency data from bytes 2 and 3 is stored in a 15-bit shift register and is used to control the division ratio of the 15-bit programmable divider which is preceded by a divide-by-16 prescaler and amplifier to give excellent sensitivity at the local oscillator input; see Fig 5. The input impedance is shown in Fig 7.

The programmed frequency can be calculated by multiplying the programmed division ratio by 16 times the comparison frequency F_{comp}.

When frequency data is entered, the phase comparator, via the charge pump and varactor drive amplifier, adjusts the local oscillator control voltage until the output of the programmable divider is frequency and phase locked to the comparison frequency.

The reference frequency may be generated by an external source capacitively coupled into pin 2 or provided by an on-board 4MHz crystal controlled oscillator.

Note that the comparison frequency is 7·8125kHz when a 4MHz reference is used.

Bit 2 of byte 4 of the programming data (CP) controls the current in the charge pump circuit, a logic 1 for ±170µA and a logic 0 for ±50µA, allowing compensation for the variable tuning slope of the tuner and also to enable fast channel changes over the full band. Bit 4 of byte 4 (T0) disables the charge pump if set to a logic 1. Bit 8 of byte 4 (OS) switches the charge pump drive amplifier's output off when it is set to a logic 1. Bit 3 of Byte 4 (T1) selects a test mode where the phase comparator inputs are available on P6 and P7, a logic 1 connects F_{comp} to P6 and F_{div} to P7.

Byte 5 programs the output ports P0 to P7; on a logic 0 for a high impedance output, logic 1 for low impedance (on).

READ MODE

When the device is in the read mode the status data read from the device on the SDA line takes the form shown in Table 2.

Bit 1 (POR) is the power-on reset indicator and is set to a logic 1 if the power supply to the device has dropped below 3V and the programmed information lost (e.g., when the device is initially turned on). The POR is set to 0 when the read sequence is terminated by a stop command. The outputs are all set to high impedance when the device is initially powered up. Bit 2 (FL) indicates whether the device is phase locked, a logic 1 is present if the device is locked and a logic 0 if the device is unlocked.

Bits 3, 4 and 5 (I2,I1,I0) show the status of the I/O Ports P7, P5 and P4 respectively. A logic 0 indicates a low level and a logic 1 a high level. If the ports are to be used as inputs they should be programmed to a high impedance state (logic 1). These inputs will then respond to data complying with TTL type voltage levels. Bits 6, 7 and 8 (A2,A1,A0) combine to give the output of the 5 level ADC.

The 5 level ADC can be used to feed AFC information to the microprocessor from the IF section of the receiver, as illustrated in the typical application circuit.

APPLICATION

A typical Application is shown in Fig. 4. All input/output interface circuits are shown in Fig. 6.

	MSB							LSB		
Address	1	1	0	0	0	MA1	MA0	0	A	**Byte 1**
Programmable divider	0	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	A	**Byte 2**
Programmable divider	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}	A	**Byte 3**
Charge pump and test bits	1	CP	T1	T0	1	1	1	OS	A	**Byte 4**
I/O port control bits	P7	P6	P5	P4	P3	X	X	P0	A	**Byte 5**

Table 1 Write data format (MSB transmitted first)

Address	1	1	0	0	0	MA1	MA0	1	A	**Byte 1**
Status byte	POR	FL	I2	I1	I0	A2	A1	A0	A	**Byte 2**

Table 2 Read data format (MSB is transmitted first)

A	:	Acknowledge bit
MA1, MA0	:	Variable address bits (see Table 4)
CP	:	Charge Pump current select
T1	:	Test mode selection
T0	:	Charge pump disable
OS	:	Varactor drive Output disable Switch
P7, P6, P5, P4, P3, P0	:	Control output states
POR	:	Power On Reset indicator
FL	:	Phase lock detect flag
I2, I1, I0	:	Digital information from Ports P7, P5 and P4, respectively
A2, A1, A0	:	5 Level ADC data from P6 (see Table 3)
X	:	Don't care

A2	A1	A0	Voltage input to P6
1	0	0	$0.6V_{CC}$ to 13.2V
0	1	1	$0{\cdot}45V_{CC}$ to $0{\cdot}6V_{CC}$
0	1	0	$0{\cdot}3V_{CC}$ to $0{\cdot}45V_{CC}$
0	0	1	$0{\cdot}15V_{CC}$ to $0{\cdot}3V_{CC}$
0	0	0	0 to $0.15V_{CC}$

Table 3 ADC levels

MA1	MA0	Voltage input to P3
0	0	0V to $0{\cdot}2V_{CC}$
0	1	Always valid
1	0	$0{\cdot}3V_{CC}$ to $0{\cdot}7V_{CC}$
1	1	$0{\cdot}8V_{CC}$ -13.2V

Table 4 Address selection

Fig. 3 Data formats

APPLICATION

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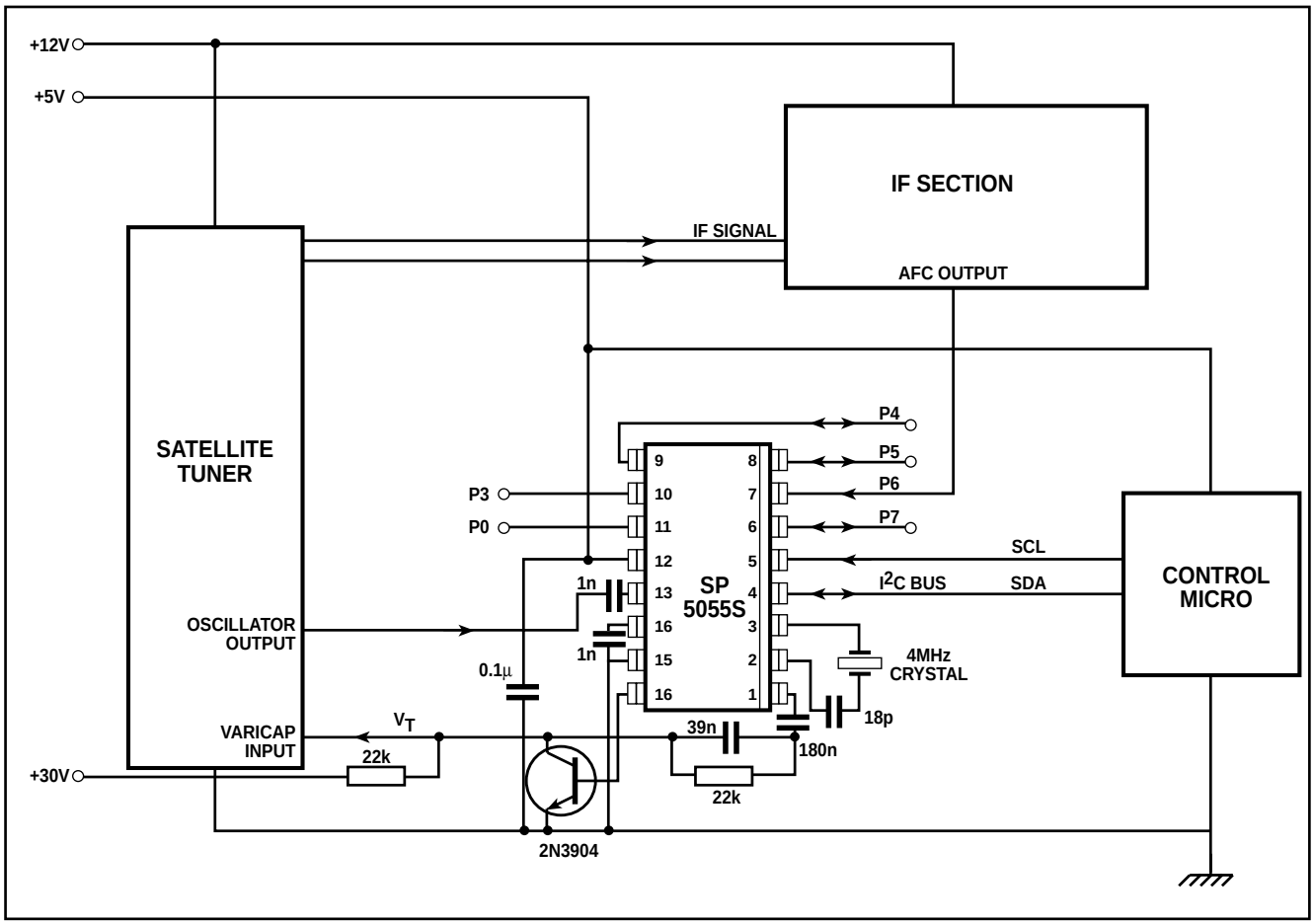


Fig. 4 Typical application

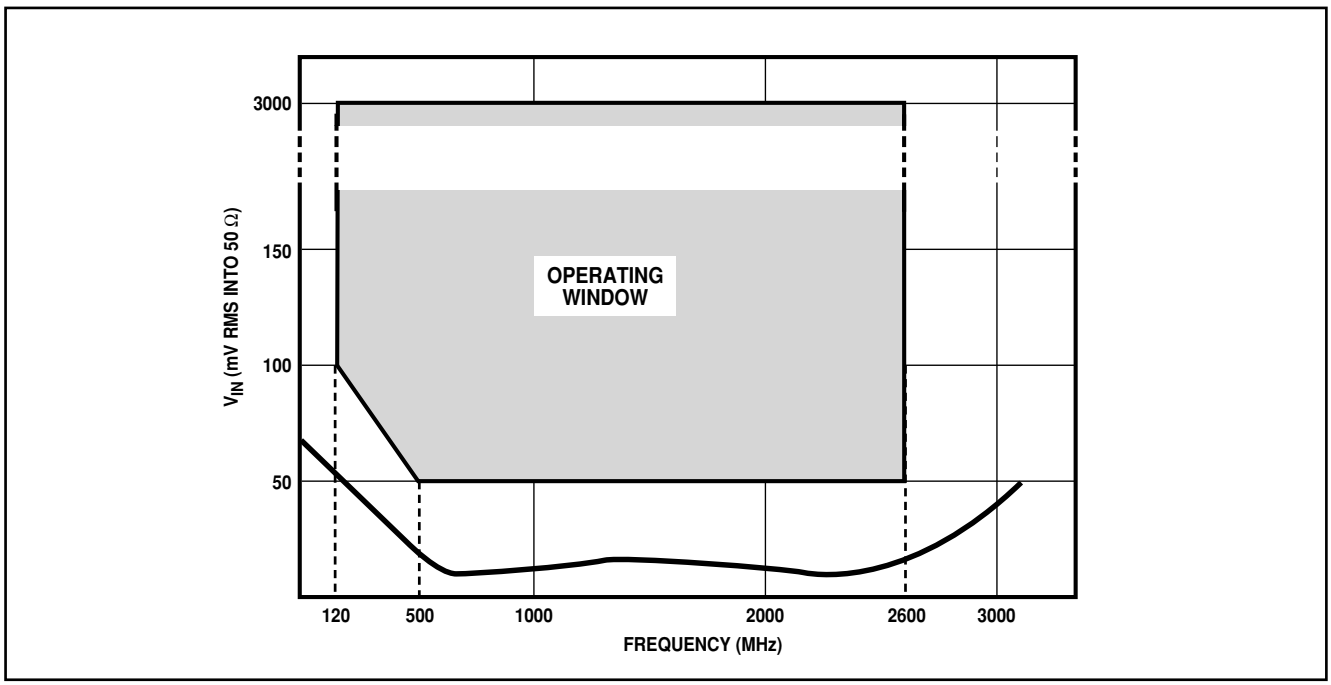


Fig. 5 Typical input sensitivity

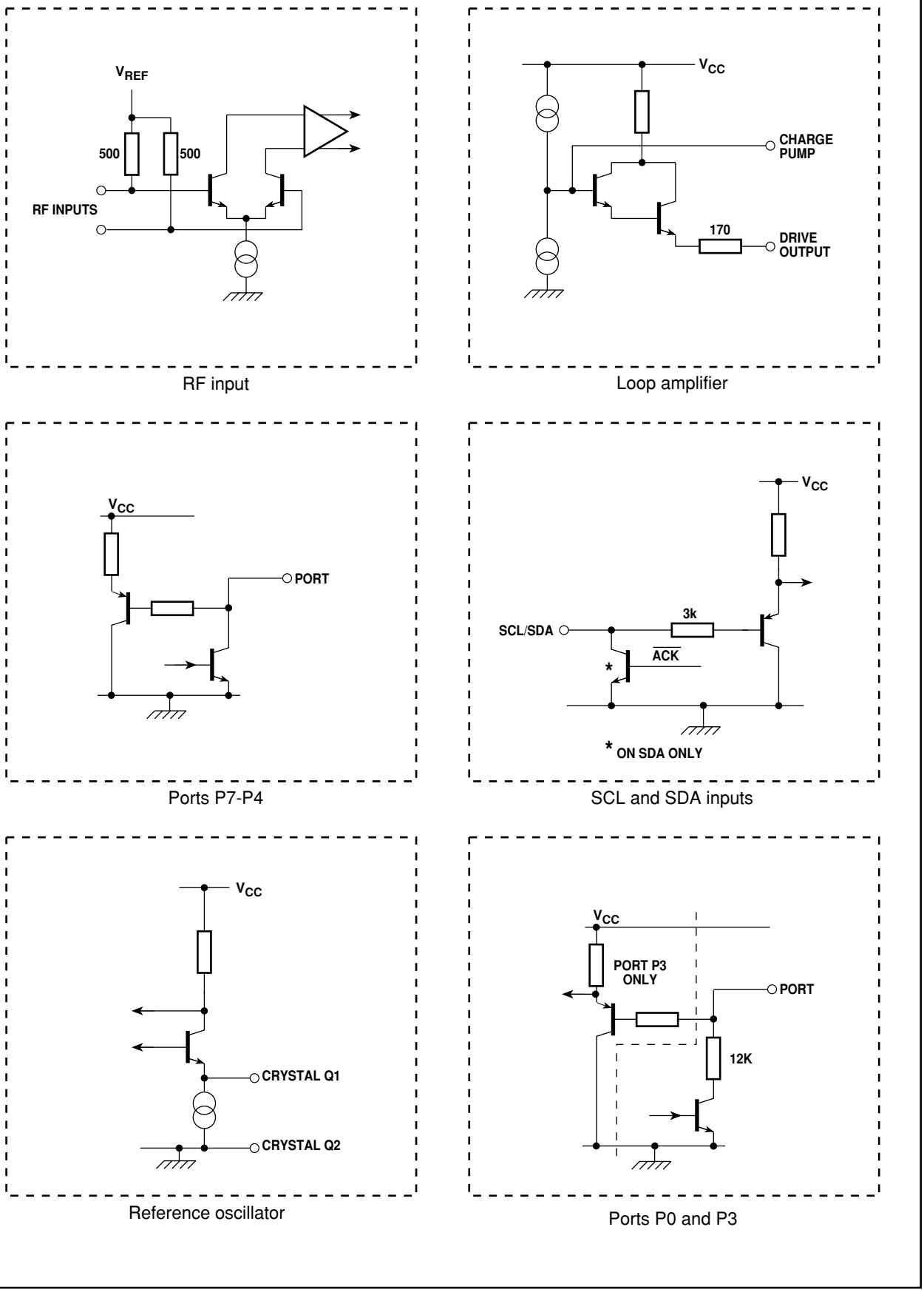


Fig. 6 SP5055 Input/output interface circuits

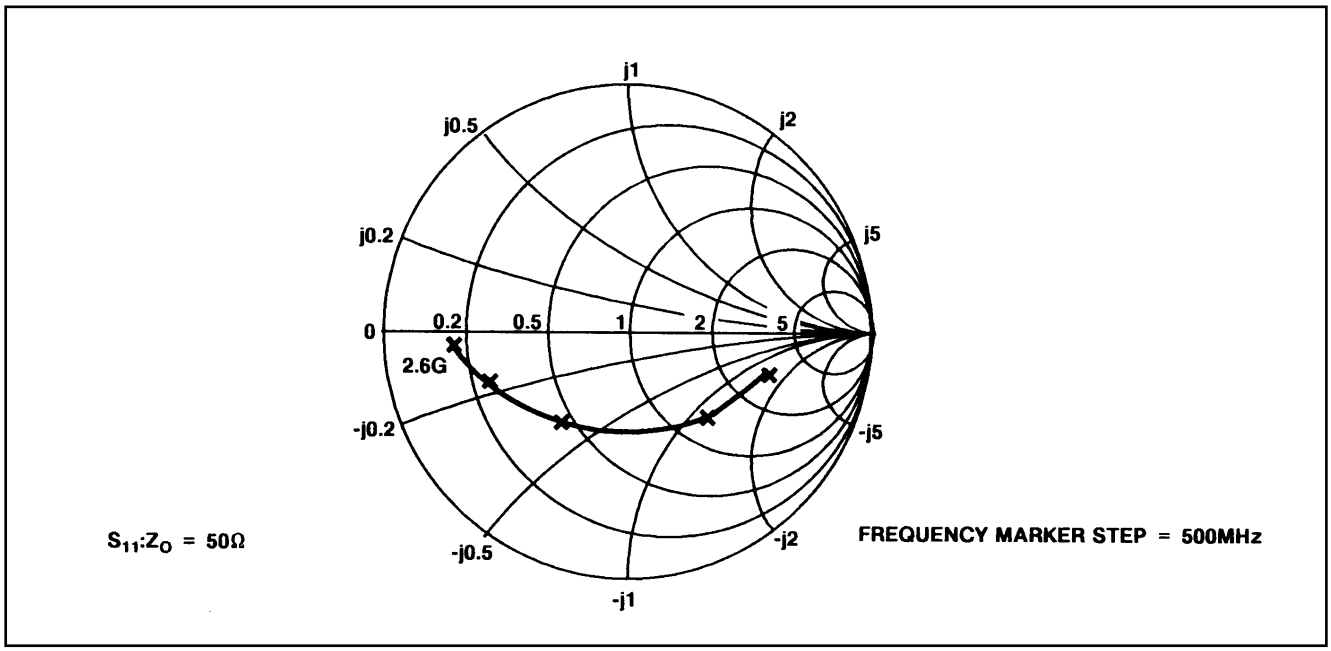
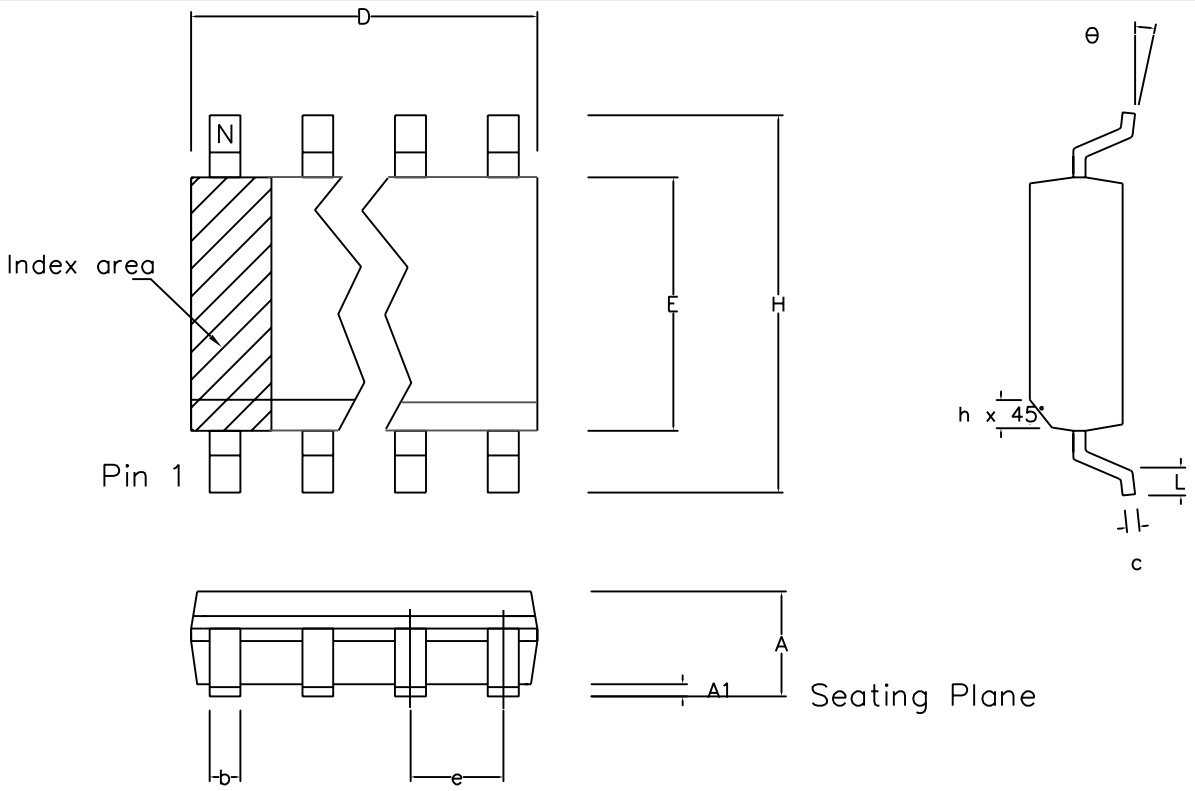


Fig. 7 Typical input impedance

ABSOLUTE MAXIMUM RATINGS

All voltages are referred to V_{EE} and pin 3 at 0V

Parameter	Pin	Value		Units	Conditions
		Min.	Max.		
Supply voltage	12	-0.3	7	V	
RF input voltage	13, 14		2.5	Vp-p	
Port voltage	6-11	-0.3	14	V	Port in off state
	6-9	-0.3	6	V	Port in on state
	10, 11	-0.3	14	V	Port in on state
Total port output current	6-11		50	mA	
RF input DC offset	13, 14	-0.3	V_{CC}+0.3	V	
Charge pump DC offset	1	-0.3	V_{CC}+0.3	V	
Drive DC offset	16	-0.3	V_{CC}+0.3	V	
Crystal oscillator DC offset	2	-0.3	V_{CC}+0.3	V	
SDA, SCL input voltage	4, 5	-0.3	V_{CC}+0.3	V	With V_{CC} applied
		-0.3	5.5	V	V_{CC} not applied
Storage temperature		-55	+125	°C	
Junction temperature			+150	°C	
MP 16 Thermal resistance, chip-to-ambient			111	°C/W	
MP 16 Thermal resistance, chip-to-case			41	°C/W	
Power consumption at 5.5V			440	mW	All ports off



	Min mm	Max mm	Min inch	Max inch
A	1.35	1.75	0.053	0.069
A1	0.10	0.25	0.004	0.010
D	9.80	10.00	0.386	0.394
H	5.80	6.20	0.228	0.244
E	3.80	4.00	0.150	0.157
L	0.40	1.27	0.016	0.050
e	1.27 BSC		0.050 BSC	
b	0.33	0.51	0.013	0.020
c	0.19	0.25	0.008	0.010
θ	0°	8°	0°	8°
h	0.25	0.50	0.010	0.020
	Pin Features			
N	16		16	
Conforms to JEDEC MS-012AC Iss. C				

Notes:

1. The chamfer on the body is optional. If not present, a visual index feature, e.g. a dot, must be located within the cross-hatched area.
2. Controlling dimensions are in inches.
3. Dimension D do not include mould flash, protusion or gate burrs. These shall not exceed 0.006" per side.
4. Dimension E1 do not include inter-lead flash or protusion. These shall not exceed 0.010" per side.
5. Dimension b does not include dambar protusion / intrusion. Allowable dambar protusion shall be 0.004" total in excess of b dimension.

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